RESUME

1. Name : SOMSUBHRA TALAPATRA
2. Address : Dept. of Electronics & Communication Engineering,
   Aliah University New Town Campus,
   Plot-IIA/27, New Town, Kolkata, PIN-700156.
   Telephone No. : +91-033-23215317. email: s_talapatra@rediffmail.com.

3. Academic Qualifications:

Examination Passed	Board/ University	Year	Div. / Class	% of Marks	Subject/ Stream	Specialization
Madhyamik Examination.	WBBSE	1992	1st Div.	83.5	Languages,Ph Sc, LSc,Maths,Mechanics, Humanities.	
Higher Secondary.	WBCHSE	1994	1st Div.	78.1	Languages,Chemistry, Physics,Maths, Biology.	
B.E.	Jadavpur University, Kolkata-32	1998	1st Class(Hons.)	84.1#	Electronics & Telecommunication Engg.	
M.E.	Jadavpur University, Kolkata-32	2005*	1st Class.	83.64	Electronics & Telecommunication Engg.	Electron Devices.

*Note: Gap in the academic career is due to work in the VLSI Industry from 1998 to 2002.

4.Details of Employment Held:
4(a) Work Experience.

Employer	Designation/	Period	Job Responsibilities.
INDUSTRIAL R&D			
Texas Instruments (India) Pvt. Ltd., Bangalore.	IC Design Enginner.	From 1st July 1998 To 6th Nov' 2002 (4 years, 4 months & 6 days)	Digital Logic Design, synthesis, physical synthesis, static timing analysis, Functional & Emulation verification using QuickTurn FPGA box, timing netlist simulation using IKOS box, etc.
TEACHING			
Purabi Das School of Information Technology, Bengal Engineering & Science University, Shibpur, Howrah-71103	Lecturer.	From 19th August 2005 To 19th August 2009 (4 years).	Teaching in the School of I.T. and the School of VLSI.
SMDP-II Project, School of VLSI Technology, Bengal Engineering & Science University, Shibpur, Howrah-71103	Project Faculty (Lecturer)	From 20th October 2009 To.30st June, 2012 (2 year 8 months)	Teaching in the School of VLSI Technology.
Dept. of Electronics & Communication	Assistant Professor,	From 12th July, 2012 till date	Teaching and administrative duties.

Engg., Aliah University, New Town Campus, Kolkata-700156.	Level-I (Since Joining)	(6 years 1 months)	

4(b) Industrial R&D Projects worked in:

- Developer, Development of Random Test Program Generator (RTPG) for Texas Instruments TMS320C27x DSP in PERL, Texas Instruments Pvt. Ltd., Bangalore, 1998.
- Team member, Development Trace Data Export Peripheral Block for C27x-emulation chip (Ankur-E4), Texas Instruments Pvt. Ltd., Bangalore, 1998-1999.
- Team member, Development ISA-independent Scalable and Configurable Trace Data Export Receiver Chip (Drishti), Texas Instruments, Bangalore, 1999-2000.
- Team member, QuickTurn FPGA based Emulation of Trace Data Export Receiver Functional Netlist (Drishti), Texas Instruments Pvt. Ltd., Houston,Texas, U.S., 2000.
- Team member (short time involvement), Development of ISA of C28x, Texas Instruments, Bangalore, 2001.
- Team member (short time project), Development of C62x based DSL Modem (AJAX) chip, Texas Instruments, Bangalore, 2001.
- Team member (short time involvement), Development of Bi-Core (c62x DSP and MIPS) DSL Modem SoC (Sangam), Texas Instruments, Bangalore, 2001-2002.

4(c) Administrative Duties in Academics:

- Head (Officiating), Dept. of ECE, Aliah University from 13.07.2015 to 21.03.2016.
- Member of Examination Committee, Aliah University, for Three Academic Sessions 2013-14, 2014-15 and 2015-16.
- Member Board of Studies, Dept. of ECE, Aliah University.

5.Research and Teaching:

5(a) Research Interest:

- Electron Devices.
- Integrated Circuit Design
- Computer Architecture
- Finite Field Arithmetic Architectures.
- CNT based VLSI Interconnects.

5(b). Details of papers published:

Journal: 2 (including one *IEEE TVLSI*). Edited Volume: 3
International Conference: 9. National(India) Conference: 3
Citations: 62 (www.researchgate.net)

Papers in Journals:

1. **Somsubhra Talapatra**, Hafizur Rahaman, and Jimson Mathew "Low Complexity Digit Serial Systolic Montgomery Multipliers for Special Class of GF(2^m)," *IEEE Trans. VLSI Syst.*, vol. 18(5), pp. 847- 852, May. 2010.

2. Sudip Ghosh, **Somsubhra Talapatra**, Navonil Chatterjee, Santi P Maity and Hafizur Rahaman, "FPGA based Implementation of Embedding and Decoding Architecture for Binary Watermark by Spread Spectrum Scheme in Spatial Domain," *Bonfring International Journal of Advances in Image Processing*, vol. 2, no. 4, pp. 1-8, December 2012.

Papers in Edited Volume:

3. Prasenjit Ray, **Somsubhra Talapatra**, and Hafizur Rahaman, "Low Latency LSB First Bit-Parallel Systolic Multiplier over GF(2m)", in Progress in VLSI Design and Test (Ed. C. P. Ravikumar), Elite Publishing, New Delhi, pp.163-172, July 2008.

4. Sudip Ghosh, **Somsubhra Talapatra**, Debasish Mondal, Navonil Chatterjee, Hafizur Rahaman, and Santi P. Maity, " VLSI Architecture for Spatial Domain Spread Spectrum Image Watermarking Using Gray-Scale Watermark," Progress in VLSI Design and Test (LNCS vol. 7373) (Eds. Sanatan Chattopadhyay *et. al.*), Springer Berlin Heidelberg, Berlin, pp. 375-376, July 2012.

5. Sudip Ghosh, **Somsubhra Talapatra**, Jayasree Sharma, Navonil Chatterjee, Hafizur Rahaman, and Santi P Maity, "Dual Mode VLSI Architecture for Spread Spectrum Image Watermarking using Binary Watermark," 2nd International Conference on Communication, Computing & Security (ICCCS-2012), Procedia Technology (Eds: Sanjay Kumar Jena and Banshidhar Majhi), Elsevier, vol. 6, pp. 784 – 791, October 2012.

Papers in International Conferences:

6. Co-Author, "Challenges in the Design of a Scalable Data-Acquisition and Processing Systems-on-Silicon," *ASP-DAC/VLSI Design 2002* ,pp: 781-788, 2002.

7. **Somsubhra Talapatra,** and Hafizur Rahaman, "Unified Digit Serial Systolic Montgomery Multiplication Architecture for Special Classes of Polynomials over GF(2^m)," 13th EUROMICRO Conf. on Digital System Design (DSD-2010), France, September 2010.

8. Sudip Ghosh, **Somsubhra Talapatra**, Hafizur Rahaman, and Shanti P. Maity, "A Novel VLSI Architecture for Walsh-Hadamard Transform", Asia Symposium on Quality Electronic Design (ASQED-2010), Malaysia, August 2010.

9. **Somsubhra Talapatra**, and Hafizur Rahaman, "Low Complexity Montgomery Multiplication Architecture for Elliptic Curve Cryptography over GF(p^m)", 18th IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC-2010), Spain, September 2010.

10. Sabir Ali Mondal, **Somsubhra Talapatra**, and Hafizur Rahaman, "Analysis, Modeling and Optimization of Transmission Gate Delay," Asia Symposium on Quality Electronic Design (ASQED-2011), Malaysia, July 2011.

11. Sudip Ghosh, **Somsubhra Talapatra**, Debasish Mondal, Navonil Chatterjee, Hafizur Rahaman, and Santi P Maity, International Conference on Advances in Computing and Communications (ICACC-2012), August 2012.

12. Sudip Ghosh, **Somsubhra Talapatra,** Sudipta Chakraborty, Navonil Chatterjee, Hafizur Rahaman, and Santi P Maity, "VLSI Architecture for Spread Spectrum Image Watermarking in Walsh-Hadamard Transform Domain using Binary Watermark," Third International Conference on Computer and Communication Technology (ICCCT), November 2012.

13. Sudip Ghosh, **Somsubhra Talapatra**,Navonil Chatterjee, Nagakumar Reddy, Santi P Maity, and Hafizur Rahaman, "Multiplier-less VLSI Architecture of 1-D Hilbert Transform pair using Biorthogonal Wavelets," International Conference on Informatics, Electronics & Vision (ICIEV), May 2013.

14. Swagata Bhattacharya ; **Somsubhra Talapatra**, "A New Walsh Hadamard Transform Architecture Using Current Mode Circuit," 2014 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 2014.

5(c). Details of M.Tech. Theses supervised:

Sl. No.	Candidates' Name	Affiliation of Candidates.	Year	Title of Theses
1	Md. Aquib	Dept. of	2018-19	Scalable VLSI Architecture for

	Javed Mallick	Electronics & Communication Engineering, Aliah University, NT Campus, Kolkata-700156.	(Work in progress)	Illumination Invariant Face Recognition in FPGA.
2	Debanjan Majumdar	Dept. of Electronics & Communication Engineering, Aliah University, NT Campus, Kolkata-700156.	2018 (Awarded)	Dynamic Multi Threshold Multivalued Logic Topology: Application to Finite Field Multiplier over GF(3^m).
3	Sabir Akhtar Mallick	Dept. of Electronics & Communication Engineering, Aliah University, NT Campus, Kolkata-700156.	2016 (Awarded)	Low Latency Digit-Serial In-Circuit Configurable Montgomery Multiplier (ICCMM) Architecture over GF(2^m) for Special Classes of Polynomials.
4	Reyaz Fahim Ansari	Dept. of Electronics & Communication Engineering, Aliah University, NT Campus, Kolkata-700156.	2015 (Awarded)	Montgomery multiplication over GF(3^m) generated by irreducible trinomial.
5	Dhanumjaya Raju Gadi	School of VLSI Design, BESU,Shibpur, Howrah-71103	2012 (Awarded)	A graph theoretical formulation for fast Montgomery multiplication in GF(2^m): Applications to digit-serial and in-circuit programmable architectures.
6	Navonil Chatterjee			VLSI architecture of spread spectrum watermarking using Walsh-Hadamard Transform and binary watermark.
7	Debasish Mondal			VLSI architecture of spatial domain image watermarking using binary watermark.
8	Jayasree Sharma			Dual mode VLSI architecture of spatial and transform domain spread spectrum image watermarking using binary watermark.
9	Dibakar Bhuiya	School of VLSI Design, BESU,Shibpur, Howrah-71103	2011 (awarded)	VLSI architecture for Hilbert transform based on bi-orthogonal wavelets
10	Sandip Mallick			Parameterized VLSI architecture for spread spectrum watermarking in Walsh transform domain
11	Samir K. Saha	School of VLSI Design, BESU,Shibpur, Howrah-71103	2010 (awarded)	Scalable latency in-circuit configurable Montgomery multiplier, using systolic cores, over GF(2^m) for special classes of polynomials.
12	Suman Dey			Modular finite field multiplier for GF(2^m).

13	Asish Bera	School of VLSI Design, BESU,Shibpur, Howrah-71103	2009 (awarded)	VLSI architectures for finite field multiplication for Elliptic Curve based cryptosystems over GF(p^m).
14	Pallab Kumar Nath			Generic fast adder structure for ast Walsh transform.
15	Manoj K. Majumder			VLSI architectures for fast Radon Transform.
16	Arijit Sarkar	Purabi Das School of IT, BESU,Shibpur, Howrah-71103		A hybrid optimization technique for efficient character recognition with emphasis on numerals.
17	Arindam Das			Optical character recognition of handwritten Bengali document.
18	Himadri Mandal	School of VLSI Design, BESU,Shibpur, Howrah-71103	2008 (awarded)	Low power high speed 16-bit Booth's Multiplier Design.
19	Swagata Bhattacharya			Walsh transform implementation using mixed signal processing.
20	Satya Gopal Dinda			Design of balanced amplitude modulator.
21	Sourav Bhattacharya	Purabi Das School of IT, BESU,Shibpur, Howrah-71103		Algorithm for geographical topology discovery by using collaborative micro-robots.
22	Sutapa Sarkar			Design, simulation and synthesis, in FPGA, of a multi-finger CDMA rake receiver using OFDM demodulator.
23	Arnab Bera			Design and hardware implementation of programmable sensor unit for wireless sensor network test infrastructure.
24	Pranab Roy	Purabi Das School of IT, BESU,Shibpur, Howrah-71103	2007 (awarded)	Study and simulation of image data compression architectures for embedded application.

BESU, Shibpur is now known as Indian Institute of Engineering, Science & Technology, Shibpur.

5(d) Journal Papers Reviewed:

I. One paper on Finite Filed Multiplier Architecture in IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Feb. 2014.
II. One paper on Finite Filed Multiplier Architecture in IEEE Transaction Very Large Scale Integration systems, Dec. 2014.

5(e) Courses Taught/Teaching:

I. VLSI Circuit Design (B.Tech., ECE,AU)
II. VLSI Circuits & Systems (M.Tech, School of VLSI Design, IIEST, Shibpur (formerly BESU))
III. Analog Integrated Circuit Design (M.Tech, School of VLSI Design, IIEST, Shibpur (formerly BESU))
IV. RFIC Design (M.Tech, School of VLSI Design, IIEST, Shibpur (formerly BESU)).
V. Semiconductor Physics and Devices (B.Tech., ECE, AU and M.Tech, School of VLSI Design, IIEST, Shibpur (formerly BESU))
VI. Memory Design (M.Tech, School of VLSI Design, IIEST, Shibpur (formerly BESU))
VII. Information Theory and Coding (B.Tech., ECE, AU and M.Tech, School of VLSI Design, IIEST, Shibpur (formerly BESU))
VIII. FPGA Architecture (M.Tech., ECE, AU)
IX. Data Structure and Algorithms (M.Tech, PDSIT, IIEST, Shibpur (formerly BESU))

X. Communication Systems and Networking (M.Tech, PDSIT, IIEST, Shibpur (formerly BESU))

5(f). Participation in Workshops and Courses:

I. "**Challenges in VLSI Design: Cutting edge Perspective**", July 21-25, 2008 (TEQIP), Bengal Engineering & Science University, Shibpur, Howrah-711103, W.B., India.
II. "**Advances in VLSI Signal Processing**", Dec 3-7, 2013, Dept. Of Electronics & Electrical Communication Engineering, IIT Kharagpur. 721302, W.B., India.
III. "**Fundamentals & Applications of Nanomaterials (CU119)**", January 01-12, 2018, National Institute of Technical Teachers' Training & Research (NITTTR), Salt Lake, Kolkata-700064, W.B., India.

6. Additional Remarks:

6(a). Awards,Medals,Prizes:

i) Awarded "National Scholarship" in 1997 by Director of Public Instruction ,West Bengal.
ii) Awarded 1st Prize in India region in "1997 TI-DSP Solution Challenge" by Dirctor,DSP Development,Texas Instruments Pvt. Ltd.

6(b). Scholarship: GATE scholarship from 2003 to 2005.

7.Skill set

Language : VHDL , System Verilog, C/C++.
Scripting Language: Perl.
Tool : Modelsim, Design compiler, IC compiler, Primetime, MATLAB, XST(Xilinx).
Verification language: Specman elite from verisity, System Verilog.